

FIGURE
1B

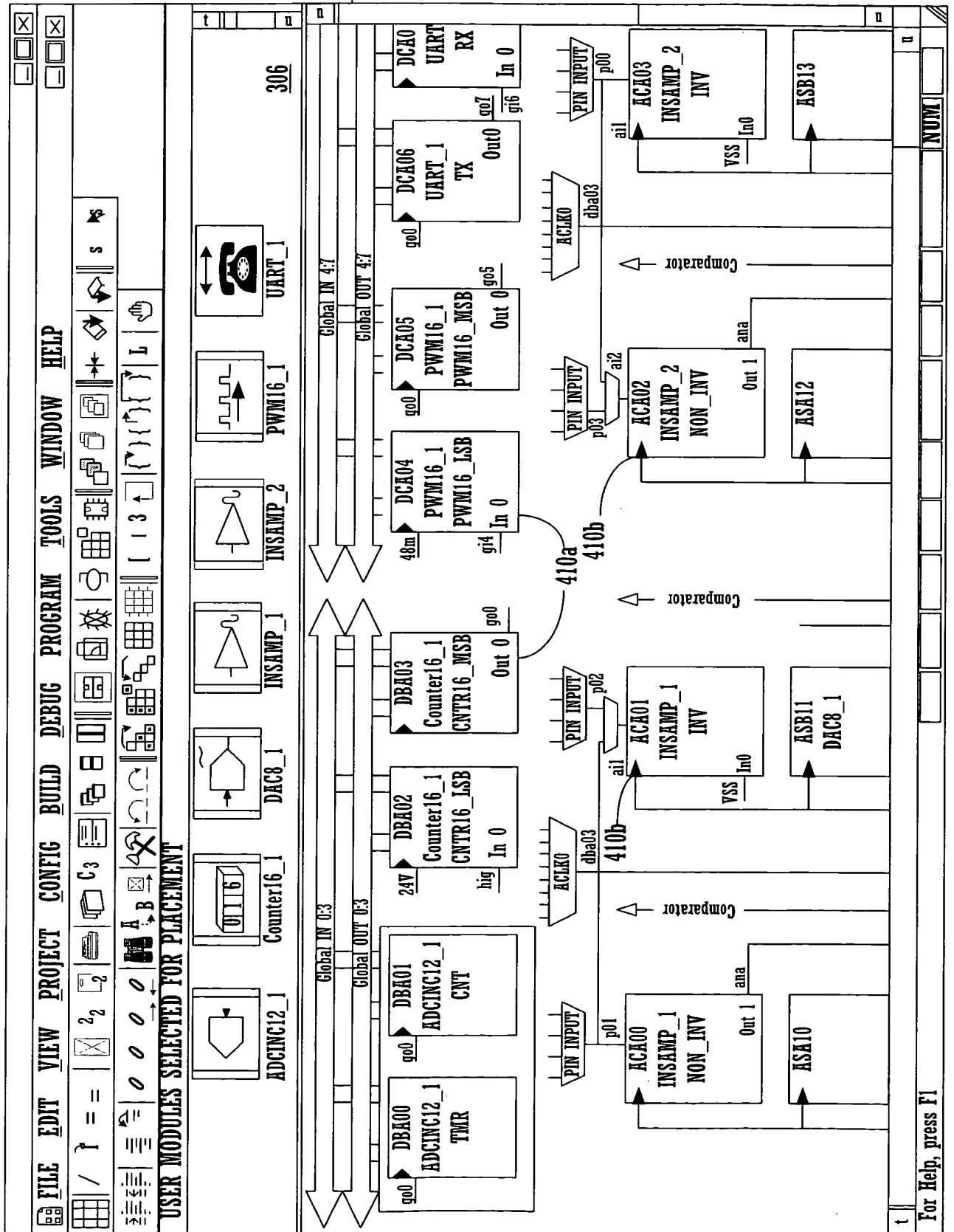
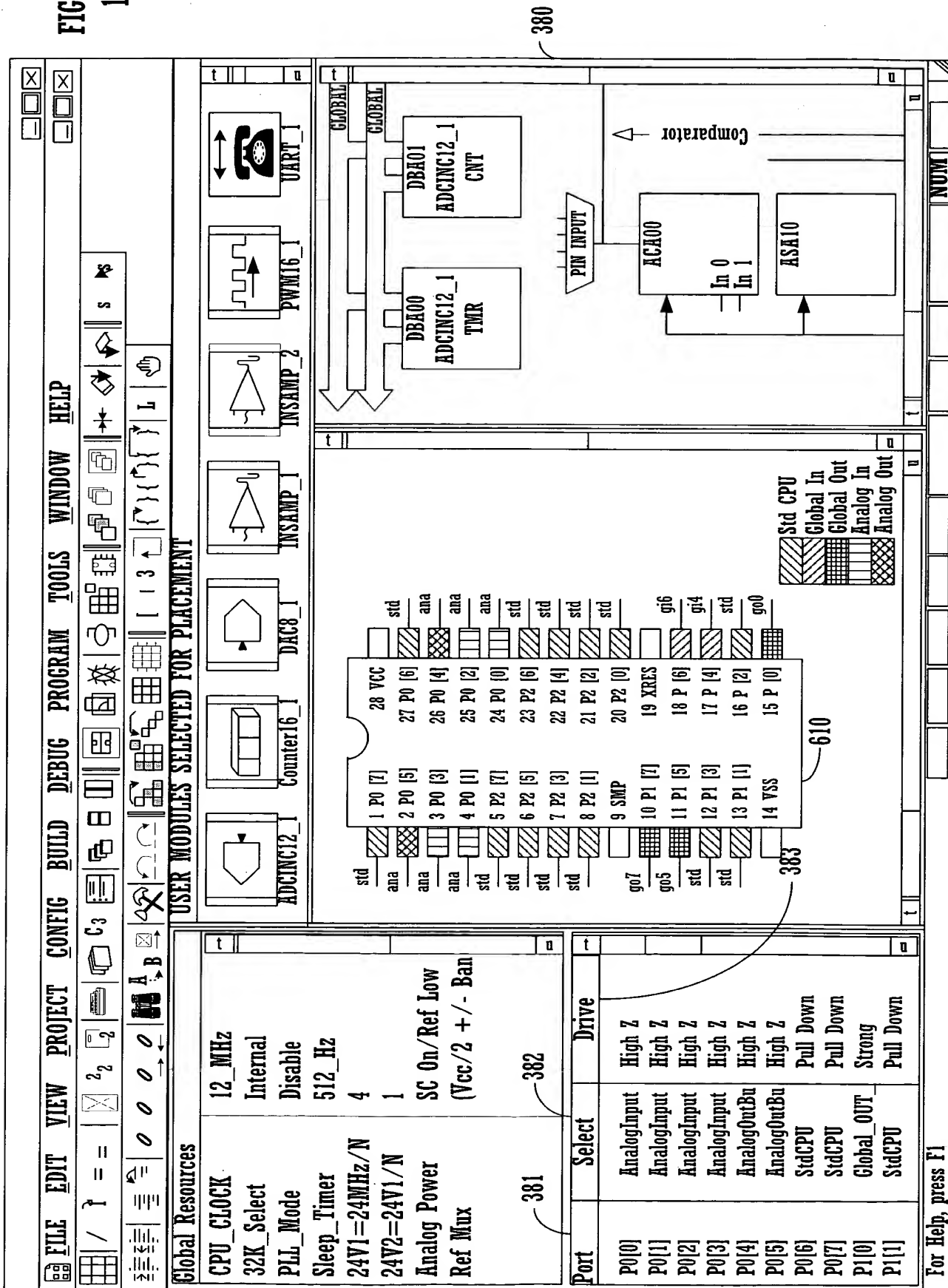


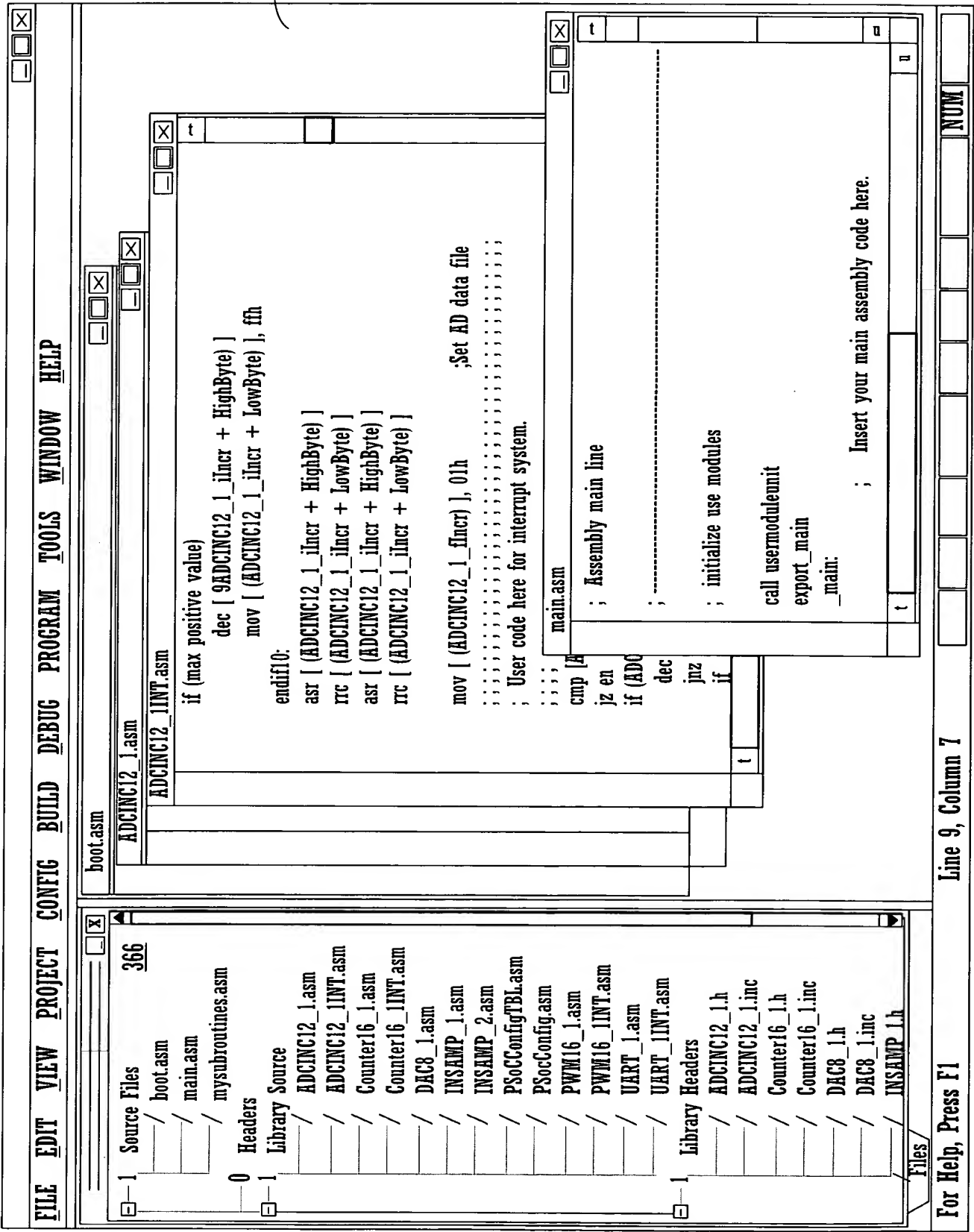
FIGURE
1C

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For Help, press F1

FIGURE
1D



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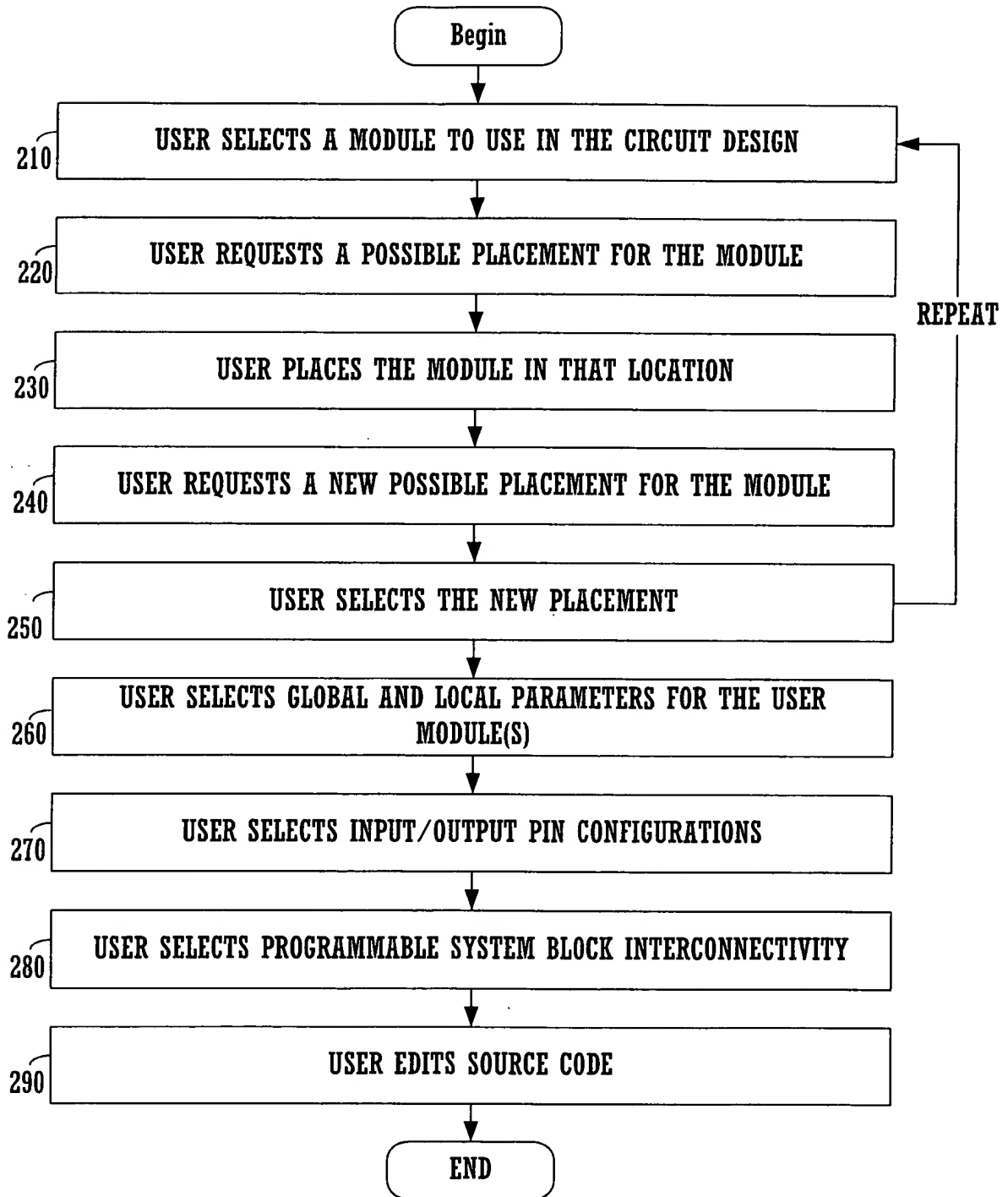
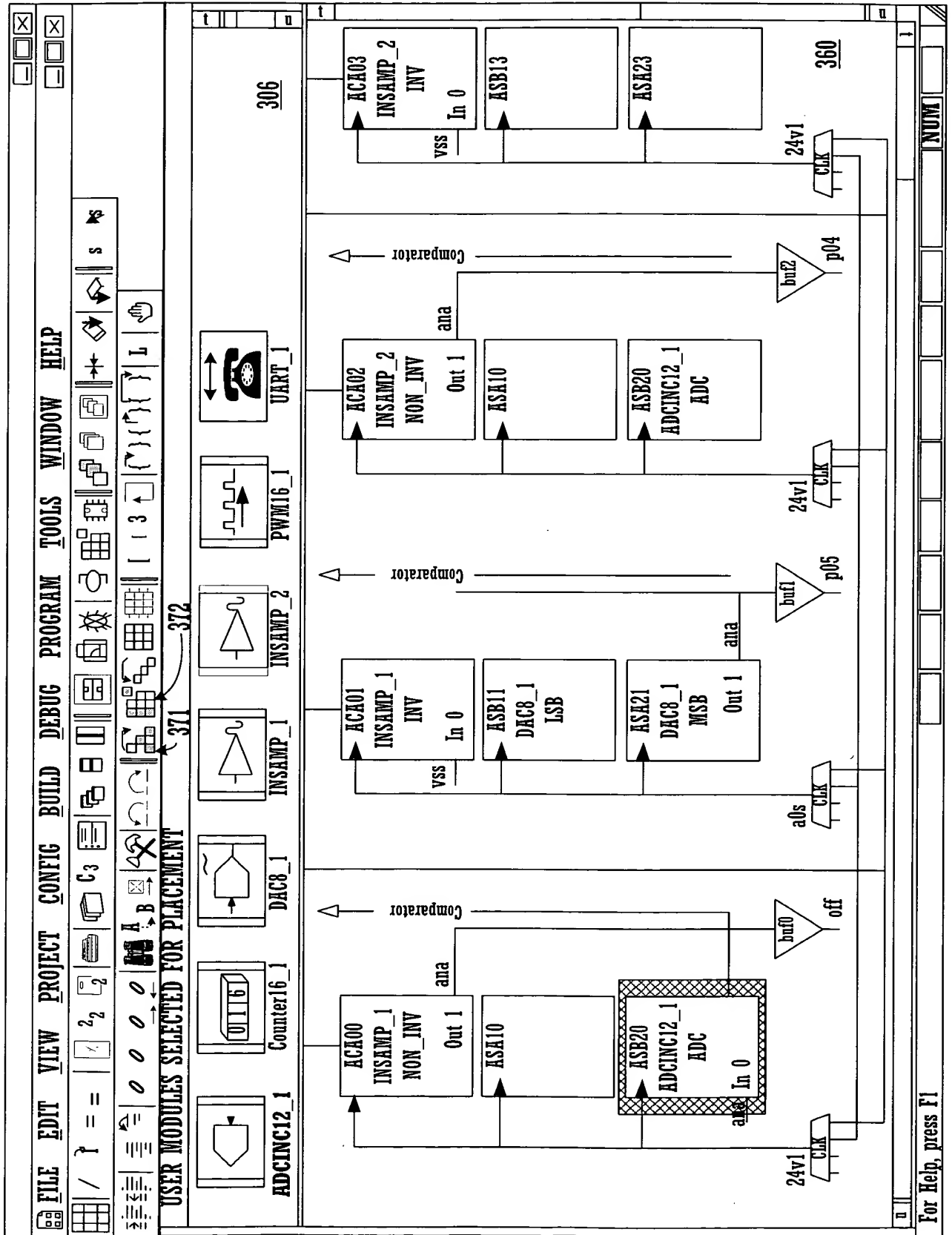


FIGURE 2

FIGURE
3A



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FIGURE
3B

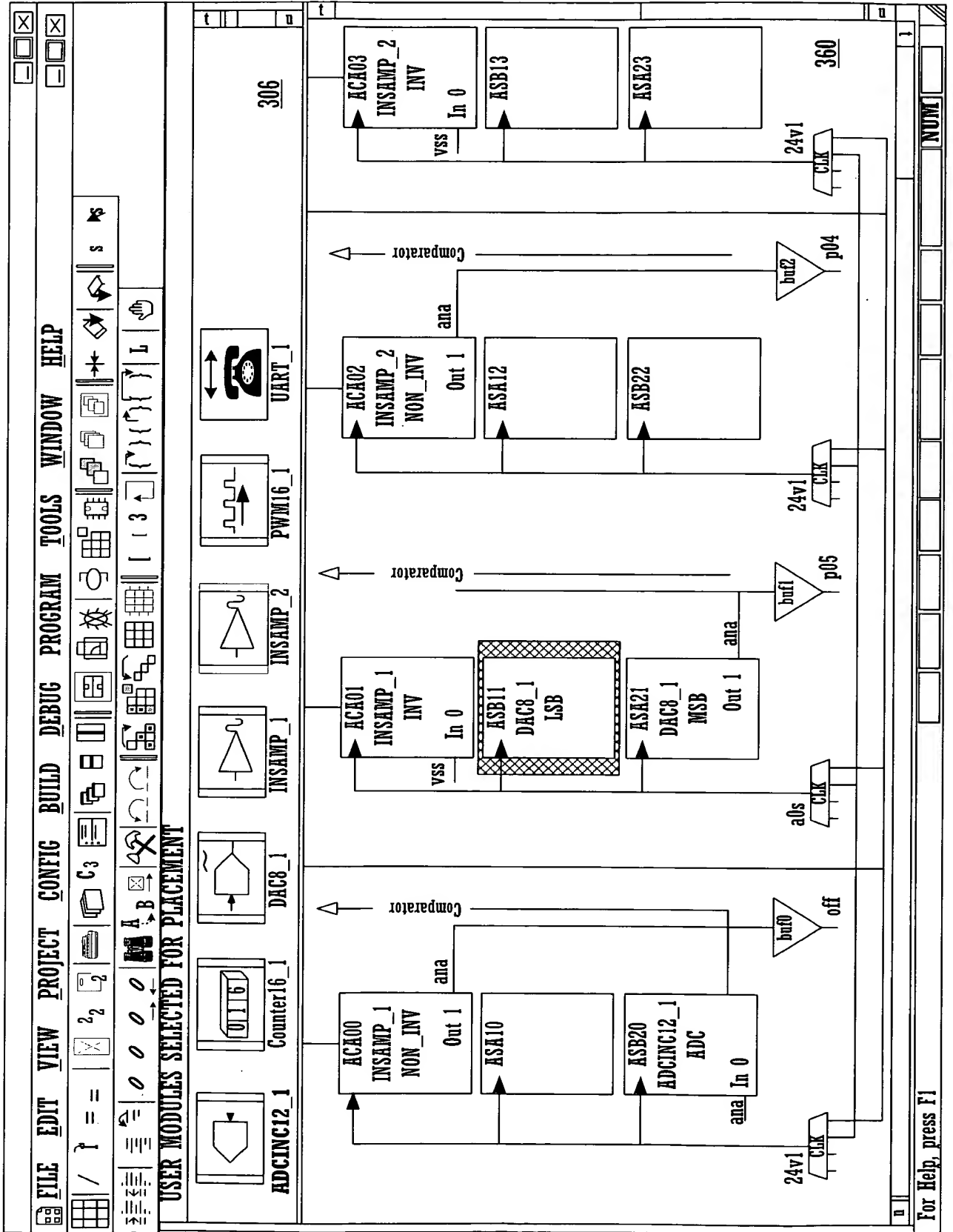
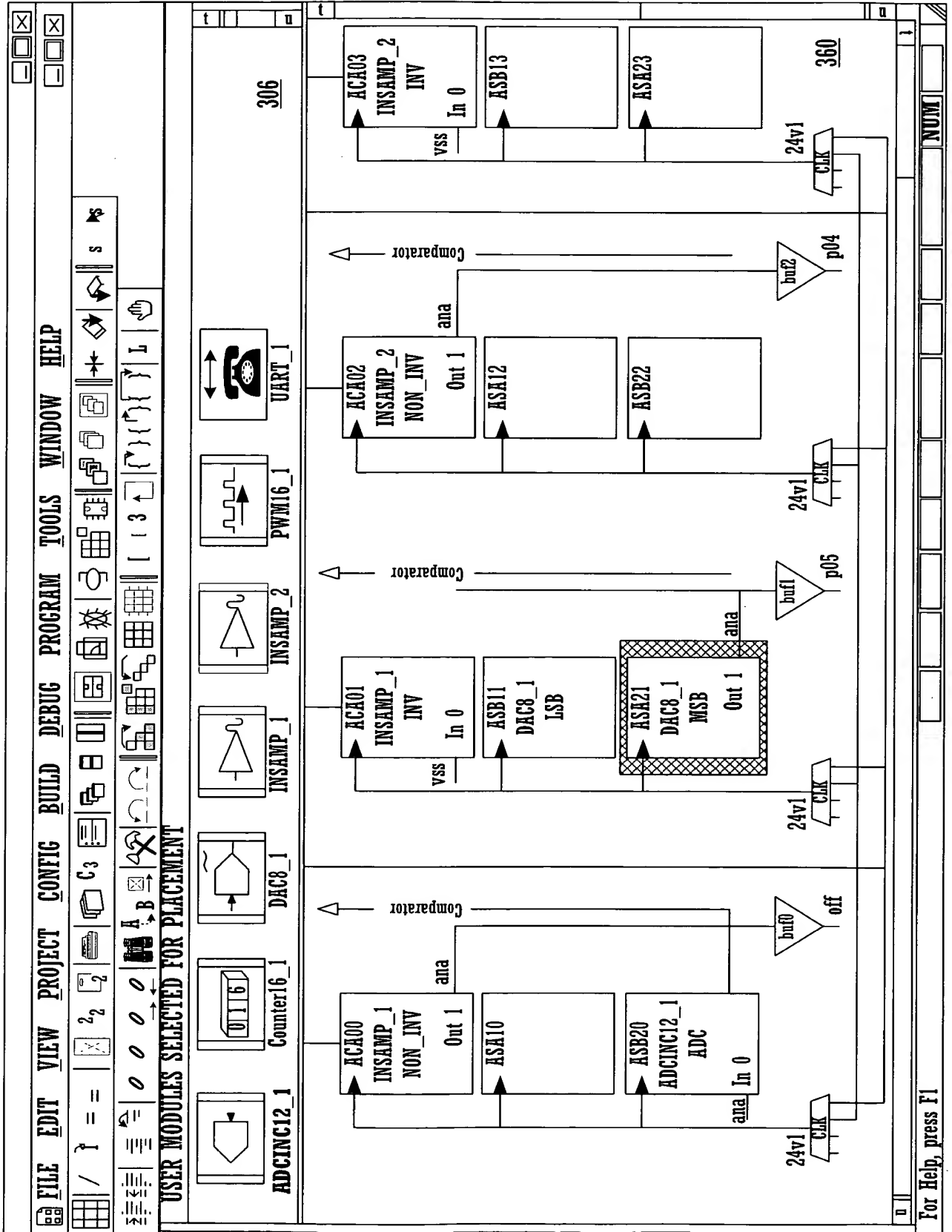


FIGURE
3C



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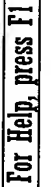
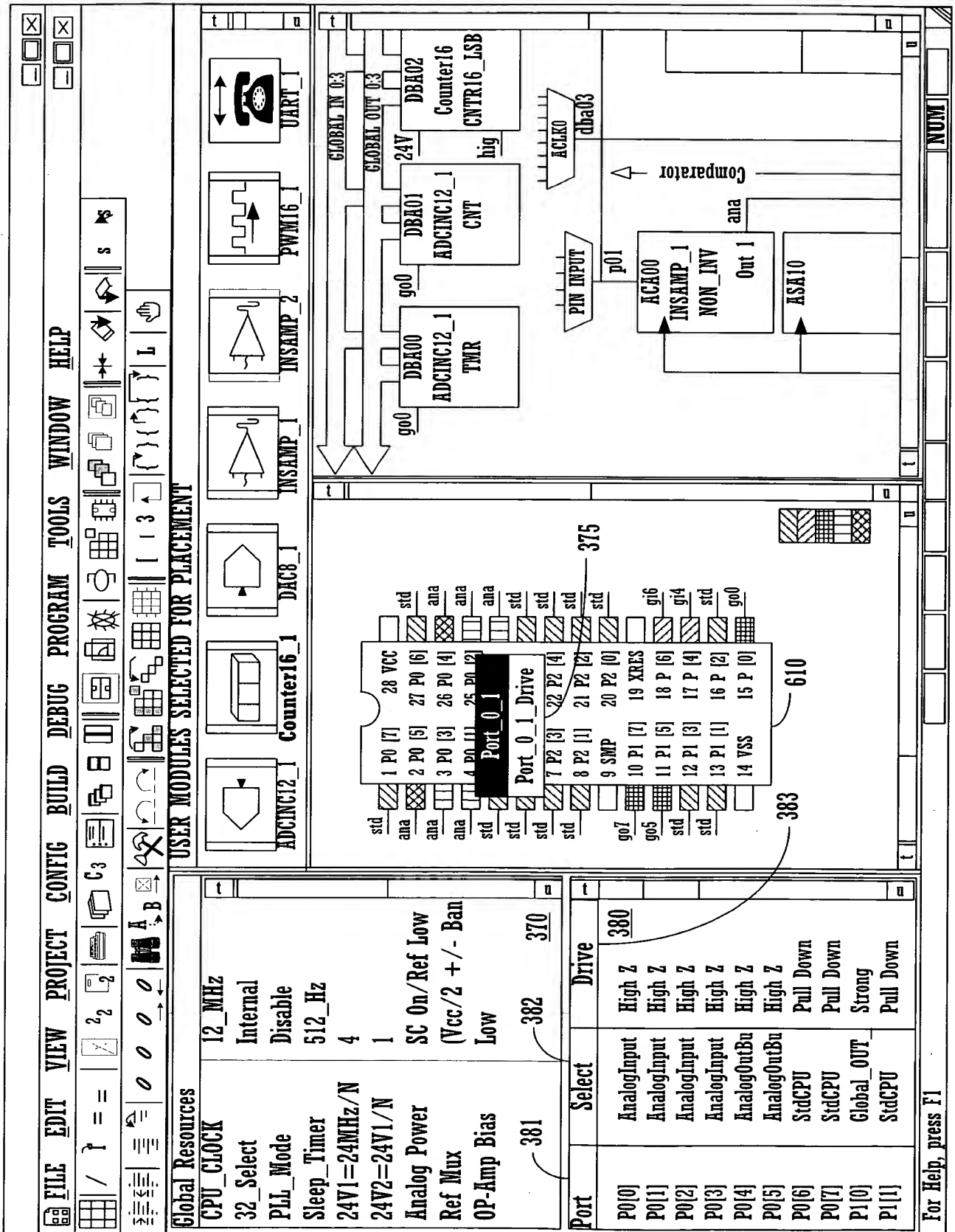


FIGURE
5A

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FIGURE
5B

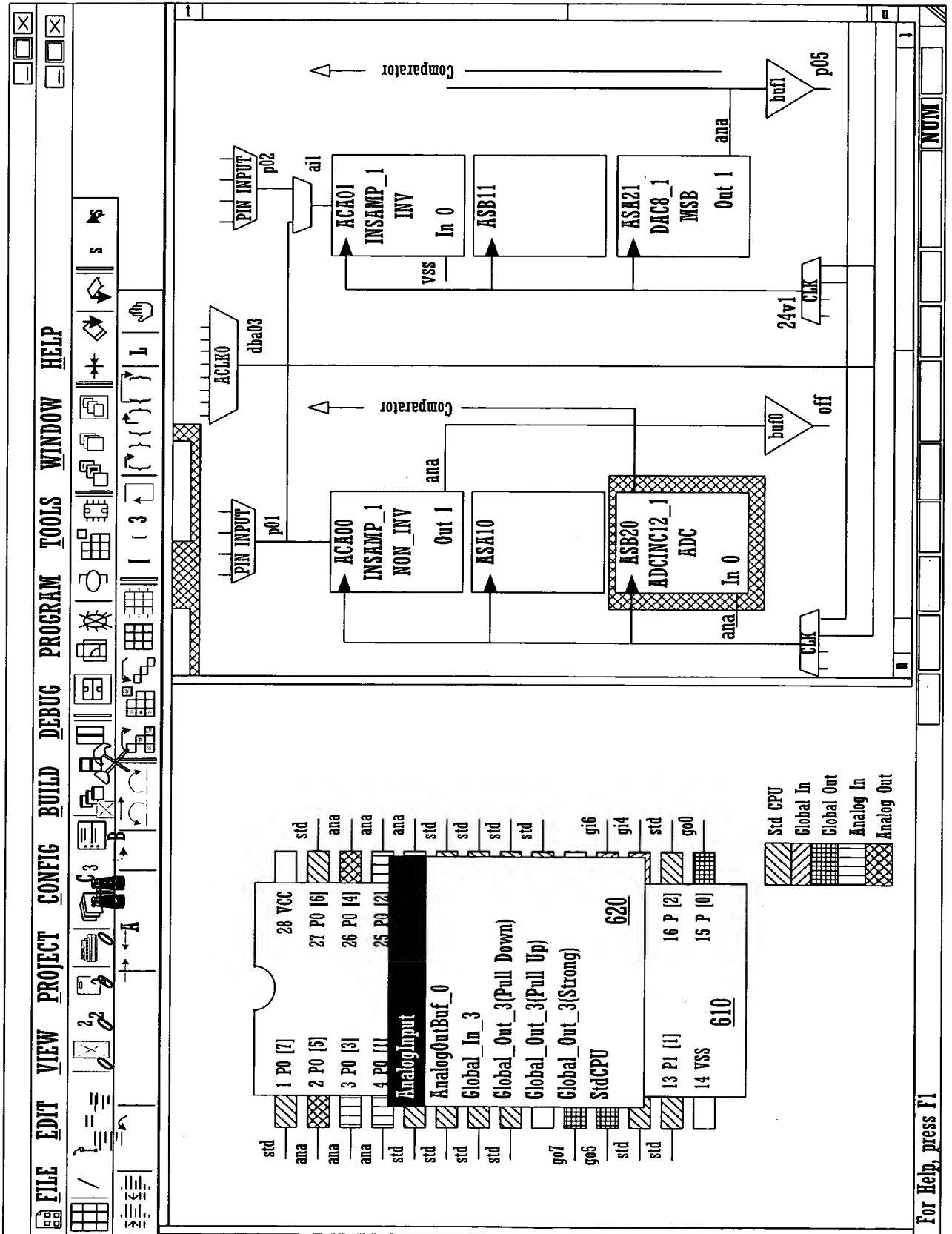
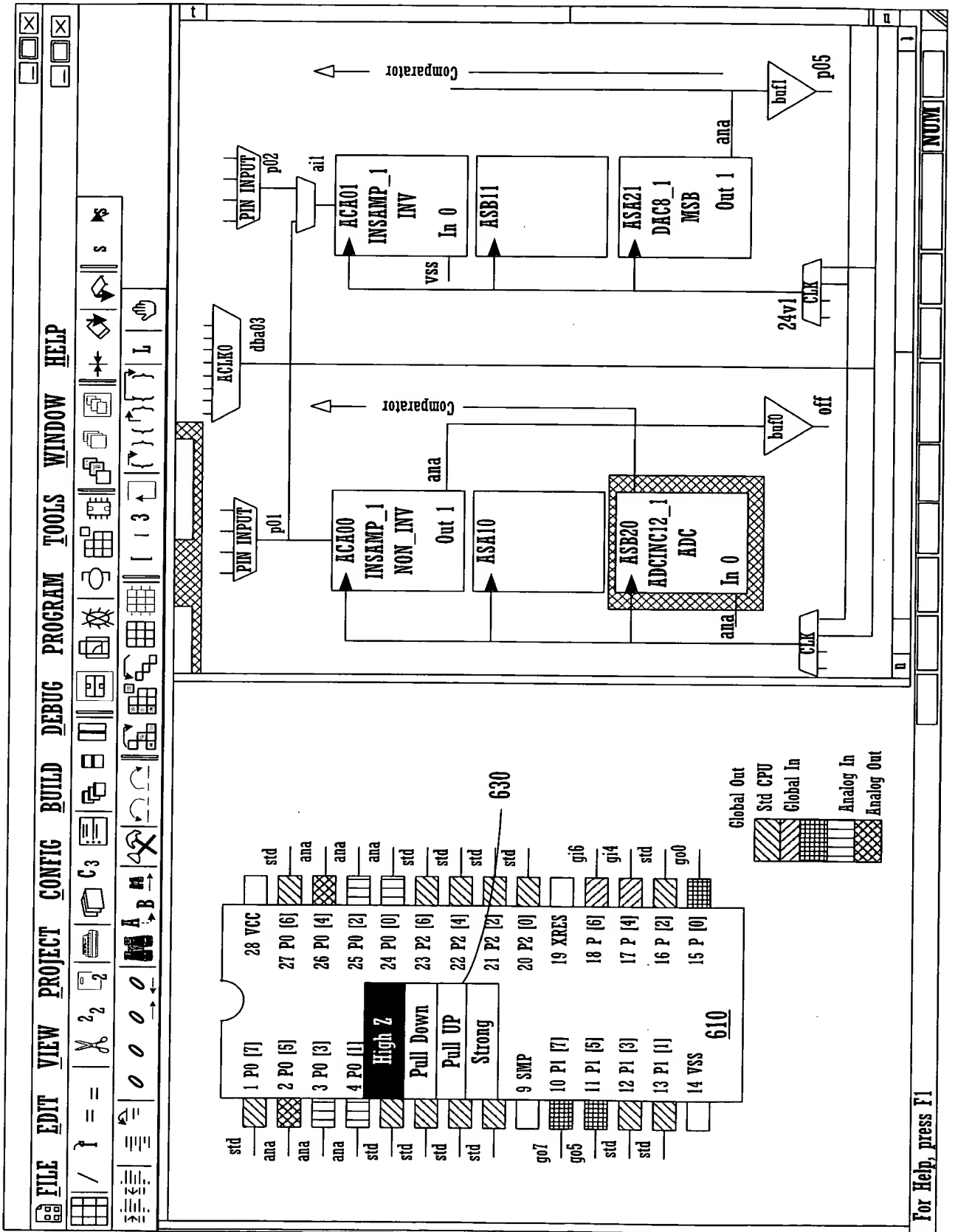


FIGURE
5C

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FILE EDIT VIEW PROJECT CONFIG BUILD DEBUG PROGRAM TOOLS WINDOW HELP

Global Resources

CPU_CLOCK	12_MHz
32_Select	Internal
Pll_Mode	Disable
Sleep_Timer	512_Hz
24V1=24MHz/N	4
24V2=24V1/N	1
Analog Power	SC On/Ref Low
Ref Mux	(Vcc/2 +/- Ban
Op-Amp Bias	Low

Port	Select	Drive
P0[0]	AnalogInput	High Z
P0[1]	AnalogInput	High Z
P0[2]	AnalogInput	High Z
P0[3]	AnalogInput	High Z
P0[4]	AnalogOutBu	High Z
P0[5]	AnalogOutBu	High Z
P0[6]	StdCPU	Pull Down
P0[7]	StdCPU	Pull Down
P1[0]	Global_OUT	Strong
P1[1]	StdCPU	Pull Down

USER MODULES SELECTED FOR PLACEMENT

ADCINC12_1

Counter16_1

DAC8_1

INSAMP_1

INSAMP_2

PWM16_1

UART_1

For Help, press F1

